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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/842,694	04/27/2001	Isao Kobayashi	35.C13077 DI	9229

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/842,694	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on th cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 7-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7,8 and 10* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement of Paper No. 2.

Drawings

1. Figures 1 – 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Response to Amendment

In response to the Supplementary Preliminary Amendment filed 06/08/01 examiner reminds Applicants that claims 4 – 6 were elected to be part of the Parent Application and hence, counter to apparent expectations of Applicants, ***claim 5*** *will not be considered in this Action, pertaining as it does to a method of making instead of a product made.*

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claims 1-3*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Takeda et al (5,591,963). Referring to Figs. 4B, 9 and 11A, and to column 7, lines 26-42, column 11, line 51 – column 12, line 4: Takeda et al teach a photoelectric converter comprising a photoelectric conversion element of a laminated structure comprising:

a first electrode layer 2;

a lower insulating layer 70 for blocking the passage of first and second carrier having different polarity from the first carrier;

a photoelectric conversion semiconductor layer 4;

an upper insulating layer or injection blocking layer 71 for blocking (a/o) the injection of the first carrier to the photoelectric conversion layer 4;

a second electrode layer in the form of transparent upper electrode 6; and, with reference to Fig. 9:

a switching means for operating the voltage, said means in the sense of Applicants' disclosure, pages 17 – 18, namely: controlled in such a manner that the switch is connected to a negative power source $V_{UB}=(V_U - V_B)$ on the refresh side 115 (cf. column 11, lines 51-59), to a positive power source on the read or photoelectric conversion side 120 (cf. column 11, line 66 – column 12, line 4);

said switching means for operating the converter by switching through the following operation modes b) through c), in that order, to apply an electric field to each layer of the photoelectric element (cf. column 13, lines 52-60):

b) a refresh mode for refreshing the first carrier accumulated in the photoelectric conversion element; and

c) a photoelectric conversion mode for generating pairs of the first carrier and second carrier in accordance with an amount of incident light to accumulate the first carrier.

While in the Example 2, Fig. 9, there is no explicit mention of an idling mode, it is obvious from Fig. 4B and the discussion of Example 1, specifically column 7, lines 40-42 that the essence of the idling mode (recess mode in Applicant's disclosure) in other embodiments of the invention by Takeda et al is present through this Example for the obvious reason to have the option of setting $V_{UB} = 0$: because this mode pertains to the relaxation of the intrinsic semiconductor layer 4 to its natural state, this setting has the obvious purpose of emitting excess carriers from the layer and hence from the photoelectric conversion element.

By combining the Examples 1 and 2 it would thus have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the complete switching means as described in claim 1, and therefore claim 1 is unpatentable over Takeda et al.

With regard to claim 2: as explained above, $V_{UB} = 0$ in the idling mode, while being positive in the photoelectric conversion mode; hence claim 2 does not distinguish over the prior art.

With regard to claim 3: in the idling mode by Takeda et al $V_{UB} = 0$, as mentioned just above. The idling mode thus complies with the requirement according to claim 3 for the reset mode as well as for the idling mode, and, consequently, the idling mode can be thought of as being split time-wise in a reset mode followed by an idling mode both

modes being in full compliance with the requirements of claim 3. Therefore, the further limitation defined by claim 3 does not distinguish over the prior art.

4. ***Claim 7*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Takeda et al in view of Furukawa et al (5,591,960) and Arita (4,740,710). As detailed above, claim 1 is anticipated by Takeda et al. Takeda et al do not specifically teach the application of the photoelectric converter such that a plurality of said photoelectric elements are arranged one-dimensionally or two-dimensionally with a switching element connected for each of the photoelectric conversion elements according to the further limitation of claim 7. However, one- and two-dimensional arrays of photoelectric elements of this kind have long been known in the art of photoelectric converter systems, as witnessed by Furukawa et al, who teach a structure consisting of a combination of pluralities of photoelectric element array sections *for the purpose of obtaining a high level signal with low noise* (cf. column 4, lines 48-55) comprising a plurality of photoelectric conversion elements, arranged two-dimensionally (cf. column 6, lines 33-37) with a switching element connected for each of the photoelectric conversion elements (cf. column 6, lines 49-56) with all the photoelectric conversion elements being divided into a plurality of n blocs (n=3, the blocks being circuit sections 1002/1102, 2002/2102, and 4002/4102; cf. column 6, lines 49-59), a light signal of all the n x m photoelectric conversion elements (m being the number of photoelectric elements in each block; undefined in claim!) divided into n=3 blocks is output (inherent in any useful application of pluralities of photoelectric converters is their output) an intersection part of the matrix wiring, which when using the photoelectric converter

taught by Takeda et al would comprise a laminated structure in which at least a first electrode layer, an insulating layer, a semiconductor layer and a second electrode layer are provided in this order. Furukawa et al do not necessarily teach that each layer of the laminated structure should be formed as prescribed by the further limitation of claim 7. However, *from a cost production point of view* it makes utter sense to form each said layer in this manner, because of ease of mass production; while Arita, in a photoelectric reading apparatus wherein a plurality of switches are each connected with one end of each of the photoelectric elements (diodes) indeed teaches (cf. column 7, lines 25-32 and Fig. 6).

It thus would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the further limitation of claim 7.

5. ***Claim 8*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Takeda et al in view of Perez-Mendez (5,596,198). Referring to Figs. 9 and 11A, column 11, line 51 – column 12, line 4, and column 13, lines 7-18: Takeda et al teach a photoelectric converter comprising a photoelectric conversion element of a laminated structure comprising:

a first electrode layer 2;

a lower insulating layer 70 for blocking the passage of first and second carrier having different polarity from the first carrier;

a photoelectric conversion semiconductor layer 4;

an upper insulating layer or injection blocking layer 71 for blocking (a/o) the injection of the first carrier to the photoelectric conversion layer 4;

a second electrode layer in the form of transparent upper electrode 6; and

a switching means for operating the voltage, said means being exactly in the sense of Applicants' disclosure, pages 17 – 18, namely: controlled in such a manner that the switch is connected to a negative power source (V_U - V_B) on the refresh side 115 (cf. column 11, lines 51-59), to a positive power source on the read or photoelectric conversion side 120 (cf. column 11, line 66 – column 12, line 4), or to GRN (ground) (cf. column 11, lines 60-65);

a switching means for operating the voltage, said means in the sense of Applicants' disclosure, pages 17 – 18, namely: controlled in such a manner that the switch is connected to a negative power source V_{UB}=(V_U - V_B) on the refresh side 115 (cf. column 11, lines 51-59), to a positive power source on the read or photoelectric conversion side 120 (cf. column 11, line 66 – column 12, line 4);

said switching means for operating the converter by switching through the following operation modes b) through c), in that order, to apply an electric field to each layer of the photoelectric element (cf. column 13, lines 52-60):

b) a refresh mode for refreshing the first carrier accumulated in the photoelectric conversion element; and

c) a photoelectric conversion mode for generating pairs of the first carrier and second carrier in accordance with an amount of incident light to accumulate the first carrier.

While in the Example 2, Fig. 9, there is no explicit mention of an idling mode, it is obvious from Fig. 4B and the discussion of Example 1, specifically column 7, lines 40-42 that the essence of the idling mode (recess mode in Applicant's disclosure) in other embodiments of the invention by Takeda et al is present through this Example for the obvious reason to have the option of setting $V_{UB} = 0$: because this mode pertains to the relaxation of the intrinsic semiconductor layer 4 to its natural state, this setting has the obvious purpose of emitting excess carriers from the layer and hence from the photoelectric conversion element.

Takeda et al do not necessarily teach the photoelectric converter to comprise a signal processing means, display means, electric transmission means and radiation source as further defined by claim 8. However, the use of signal processing for the purpose of generating corresponding image signals to various peripherals, signal recording for video/data recorder use, signal display for interactive video display are standard in the art of photoelectric imaging, as shown for instance by Perez-Mendez (cf. column 6, lines 28-36). The examiner takes official notice that the use of electrical transmission for the transmission of data to other locations for remote processing or analysis is equally standard in the field. Finally, any photoelectric converter needs a radiation source for input, hence this aspect is inherent in a photoelectric converter system.

6. ***Claim 8*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Takeda et al in view of Sashin et al (4,696,022). Referring to Figs. 9 and 11A, column 11, line 51

– column 12, line 4, and column 13, lines 7-18: Takeda et al teach a photoelectric converter comprising a photoelectric conversion element of a laminated structure comprising:

a first electrode layer 2;

a lower insulating layer 70 for blocking the passage of first and second carrier having different polarity from the first carrier;

a photoelectric conversion semiconductor layer 4;

an upper insulating layer or injection blocking layer 71 for blocking (a/o) the injection of the first carrier to the photoelectric conversion layer 4;

a second electrode layer in the form of transparent upper electrode 6; and

a switching means for operating the voltage, said means being exactly in the sense of Applicants' disclosure, pages 17 – 18, namely: controlled in such a manner that the switch is connected to a negative power source (V_U - V_B) on the refresh side 115 (cf. column 11, lines 51-59), to a positive power source on the read or photoelectric conversion side 120 (cf. column 11, line 66 – column 12, line 4), or to GRN (ground) (cf. column 11, lines 60-65);

a switching means for operating the voltage, said means in the sense of Applicants' disclosure, pages 17 – 18, namely: controlled in such a manner that the switch is connected to a negative power source V_{UB}=(V_U - V_B) on the refresh side 115 (cf. column 11, lines 51-59), to a positive power source on the read or photoelectric conversion side 120 (cf. column 11, line 66 – column 12, line 4);

said switching means for operating the converter by switching through the following operation modes b) through c), in that order, to apply an electric field to each layer of the photoelectric element (cf. column 13, lines 52-60):

b) a refresh mode for refreshing the first carrier accumulated in the photoelectric conversion element; and

c) a photoelectric conversion mode for generating pairs of the first carrier and second carrier in accordance with an amount of incident light to accumulate the first carrier.

While in the Example 2,Fig. 9, there is no explicit mention of an idling mode, it is obvious from Fig. 4B and the discussion of Example 1, specifically column 7, lines 40-42 that the essence of the idling mode (recess mode in Applicant's disclosure) in other embodiments of the invention by Takeda et al is present through this Example for the obvious reason to have the option of setting $V_{UB} = 0$: because this mode pertains to the relaxation of the intrinsic semiconductor layer 4 to its natural state, this setting has the obvious purpose of emitting excess carriers from the layer and hence from the photoelectric conversion element.

Takeda et al do not necessarily teach the photoelectric converter to comprise a signal processing means, display means, electric transmission means and radiation source as further defined by claim 8. However, the use of signal processing for the purpose of generating corresponding image signals to various peripherals, signal recording for video/data recorder use, signal display for interactive video display are standard in the art of photoelectric imaging, as shown for instance by Sashin

(4,179,100) (cf. Fig. 23 and column 15, line 64 – column 65, line 15). The examiner takes official notice that the use of electrical transmission for the transmission of data to other locations for remote processing or analysis is equally standard in the field. Finally, any photoelectric converter needs a radiation source for photon input, hence this aspect is inherent in a photoelectric converter system.

7. ***Claim 10*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Takeda et al and Sashin et al as applied claim 8 above, and further in view of Takeuchi et al (JP363250634A; no images available on the PTO Data Base). As detailed above, claim 8 is unpatentable over Takeda et al in view of Sashin et al, who, however, do not necessarily teach the use of phosphorus as a converter of wavelength of radiation as input into a photoelectric conversion element has long been known in the art as witnessed for instance by Japanese Patent to Takeuchi et al, who teach the conversion of X-rays to light in the visible range through the use of phosphorus prior to undergoing photoelectric conversion (cf. abstract and constitution).

Allowable Subject Matter

8. ***Claim 9*** *is objected to* as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: although all values of the potential V_{UB} can be obtained in the unpatentable

device of claim 2, application of positive but small values of said potential for the purpose delineated for the idling mode, i.e., for the purpose of emitting the second carrier rather than operating the photoelectric conversion element, is non-obvious and has not been found in the prior art including Takeda et al.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

(a) Matsuda, Yuji (JP406233197A), as obtained from the Derwent Data Base;

(b) Arita et al (4,703,169).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
January 19, 2002